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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/776,541
Filing Date: February 10, 2004
Appellant(s): MORAD ET AL.

Kirk A. Vander Leest
Registration No. 34,036
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/16/2011 appealing from the Office action mailed 11/16/2011.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The application 10/170,019 is awaiting decision by the board of appeals.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

10-36.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN

REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

US 5,825,430	Adolph et al.	10-1998
US 6,490,250	Hinchley et al.	12-2002
US 6,516,031	Ishihara et al.	02-2003
US 5,448,310	Kopet et al.	09-1995
US 6,665,872	Krishnamurthy et al.	12-2003
US 6,519,289	Bruck	02-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10-20 and 24-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250).

Re claims 10 and 24, Adolph discloses an audio/video encoder device (fig. 3, a single device) comprising, on a single integrated circuit:

multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode),

which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and

which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3);

a first encoder (VE1 and AE1 of fig. 3) that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder (VE2 and AE2 of fig. 3) that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

wherein the device (fig. 3) transmits the first multiplexed stream (the output of MUX1, MUX1 of fig. 3)) to circuitry external (fig. 4) to the device (fig. 3) via a first output of the device (MOD and BBRF of fig. 3, transmitting the first output of the device (fig. 3)); and

wherein the device (fig. 3) transmits the second multiplexed stream (the output of MUX2, MUX2 of fig. 3) to circuitry external (fig. 4) to the device (fig. 3) via a second output of the device (MOD and BBRF of fig. 3, transmitting the second output (the output of MUX2) to the DMUX of fig. 4).

It is noted that Adolph does not particularly teach a single chip comprises the multiplexer, encoders, and control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder as claimed.

Hinchley teaches a single chip (120 of fig. 1) comprises the multiplexer (204 of fig. 2), encoders (208 of fig. 2), and control circuitry (250 of fig. 2) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (212, 214, 216, 218, and 220 of fig. 2).

Taking the teachings of Adolph and Hinchley as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Hinchley into the system of Adolph to efficiently multiplex the incoming streams together and flexible to adjust the data rate for different formats.

Re claim 11, Adolph further discloses wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder (VE1 and AE1, VE2 and AE2 of fig. 3).

Re claims 12 and 25, Adolph further discloses wherein the first encoder and the second encoder operate concurrently (VE1, AE1, VE2, and AE2 of fig. 3, in parallel).

Re claims 13 and 26, Adolph modified by Hinchley, Hinchley further teaches wherein the first encoder and the second encoder inherently perform luminance and chrominance filtering *(note MPEG-1 and MPEG-2 video/audio compression standards. Hence, a data block represents a macroblock, which is a sixteen by sixteen matrix of luminance pixels and two, four or eight, by*

eight matrices of chrominance pixels as defined by MPEG standards, wherein luminance and chrominance are 4:2:0, 4:2:2, or 4:4:4 as shown in Hinchley, col. 3, lines 30-38).

Re claims 14 and 27, Adolph modified by Hinchley, Hinchley further wherein the device comprises at least one interface (122 of fig. 1) for direct connection to external memory devices (108 and 116 of fig. 1) used as one or both of a frame buffer and/or an output buffer for compressed data.

Re claims 15 and 28, Adolph modified by Hinchley, Hinchley further teaches wherein the device comprises at least one bus interface (122 of fig. 1) that is configurable to operate to couple the control circuitry (250 of fig. 1) and at least one controller external (104 of fig. 1) to the device,

wherein the at least one bus interface (122 of fig. 1) comprises inherently a plurality of separate electrical signals *(note each of the components inherently has its own electrical signal (e.g. electron, voltage, digital data). Figure 1 of Hinchley has a plurality of separate electrical elements that inherently have a plurality of separate electrical signals. It is further noted that the specification of the present invention does not particularly disclose a plurality of separate electrical signals, so the plurality of electrical signals are understood that each element has its own electrical signal as shown in fig. 1 of Hinchley, e.g. the integrated multimedia encoding system has its own electrical signal (e.g. encoded data, uncompressed data ...)).*

Re claims 16 and 29, Adolph modified by Hinchley, Hinchley further teaches wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface *(Note Hinchley teaches the unified memory module 204 receives the adjusted*

elementary streams 216, 218, the output combined data 224 as well as data streams from other data sources 236, such as from the PCI bus, through a conventional FIFO 244).

Re claims 17 and 30, Adolph modified by Hinchley, Hinchley further teaches wherein the at least one bus interface is configurable to act as a bus master (122 of fig. 1) inherently using direct memory access *(support by Larson, US 5,821,987, the vision processor 48B preferably incorporates a DMA data interface with a zero-run/amplitude encoder/decoder, fig. 1).*

Re claims 18 and 31, Adolph modified by Hinchley, Hinchley further teaches wherein the at least one bus interface (122 of fig. 1) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

Re claims 19 and 32, Adolph modified by Hinchley, Hinchley further teaches wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions *(e.g. 104 of fig. 1; note the computer system 100 has a central processing unit 104, which may execute specific programs related to multimedia processing; wherein a program inherently has microcode instructions, e.g. 606 of fig. 6; col. 5, lines 25-65)* received by the device via the at least one bus interface (122 of fig. 1, PCI bus).

Re claims 20 and 33, Adolph further wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels (V1, A1, V1, and A2 of fig. 3).

3. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) in view of Ishihara et al. (US 6,516,031).

Re claims 21-22 and 34-35, Adolph modified by Hinchey, Adolph and Hinchley further teaches the MPEG-2 encoder (208 of fig. 2 of Hinchley) that would obviously has motion estimation except a plurality of search processors for performing motion analysis in parallel, each upon a different portion of a macroblock as claimed.

However, Ishihara teaches a plurality of search processors (7 of fig. 2) for performing motion analysis in parallel, each upon a different portion of a macroblock (PE1, PE2....PE33 of fig. 7; e.g. fig. 13).

Taking the teachings of Adolph, Hinchley, and Ishihara as a whole, it would have been obvious to one of ordinary skill in the art to modify the processor array (7 of fig. 2) of Ishihara into the motion estimation of the combination of Adolph and Hinchley to provide an improvement for reducing a hardware volume.

4. Claims 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) and Ishihara et al. (US 6,516,031), and further in view of Kopet et al. (US 5,448,310).

Re claim 23, the combination of Adolph, Hinchley, and Ishihara further teaches wherein the plurality of search processors operates in parallel upon a single macroblock (e.g. figs. 9 and 10 of Ishihara) and suggests the processor performs half pixels search, except each search processor operating at a different one of a plurality of resolutions as claimed.

However, Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search

resolution (col. 2, line 50 –col. 3, line 29).

Taking the teachings of Adolph, Hinchley, Ishihara, and Kopet as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Adolph, Hinchley, and Ishihara in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

5. Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430).

Re claims 10 and 24, Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) comprising, on a single integrated circuit (fig. 3, note two and more different sub-system could be implemented on a single board, col. 20, lines 34-42):

multiplexer circuitry (308 of fig. 3) that operates in a first mode and a second mode (col. 20, lines 22-25, "multi-channel mode" would obviously suggest a first mode and a second mode), which when operating in the first mode (308 of fig. 3, the multiplexer (308) for multiplexing up to 24 different channels of transport bitstreams from the MPEG-2 encoders; col. 20, lines 10-11) produces a first multiplexed stream (fig. 5, multiplexing bitstreams and outputting a first multiplexed bitstream) from first compressed video (320 of fig. 3), first compressed audio (322 of fig. 3), second compressed video (ENCn, 320 of fig. 3), and second compressed audio (ENCn, 322 of fig. 3); and

a first encoder (306 of fig. 3) that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder (306 of fig. 3, ENCn) that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

control circuitry (304 of fig. 3, note the CPU (304) is programmable to control all elements, so the CPU would obviously synchronize all element as described in figure 3) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;

wherein the device (fig. 3, see also fig. 5) transmits the first multiplexed stream to circuitry external (506 of fig. 5, col. 20, lines 27-28) to the device via a first output of the device; and wherein the device (fig. 5) transmits the second multiplexed stream to circuitry external (506 of fig. 5; col. 20, lines 27-28) to the device via a second output of the device.

Krishnamurthy does not particularly teach **when operating in the second mode** concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio as claimed.

Adolph teaches which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

Taking the teachings of Krishnamurthy and Adolph as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Adolph into the system of

Krishnamurthy to reduce the perceptibility of errors and picture failures during the terrestrial reception of the signals.

Re claim 11, Krishnamurthy further teaches wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder (306, 320, and 322 of fig. 3; ECNn of fig. 3).

Re claims 12 and 25, Krishnamurthy further teaches wherein the first encoder and the second encoder operate concurrently (parallel encoding, 306 of fig. 3).

Re claims 15 and 28, Krishnamurthy further teaches wherein the device comprises at least one bus interface (PCI, 302 and 310 of fig. 3) that is configurable to operate to couple the control circuitry (304 of fig. 3) and at least one controller external (316 of fig. 3, downloading micro-codes for MPEG-2 encoder chip, 306 of fig. 3, col. 19, lines 22-28) to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals (PCI of fig. 3).

Re claims 16 and 29, Krishnamurthy further teaches wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface (302, PCI BUS of fig. 3).

Re claims 20 and 33, Krishnamurthy further teaches wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels (AUDIO ENC of fig.3).

Re claims 18-19, 31-32, Krishnamurthy further teaches wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one

bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

6. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430), and further in view of Bruck (US 6,519,289).

Re claims 13 and 26, Krishnamurthy does not particularly teach wherein the first video encoder and the second video encoder perform luminance and chrominance filtering.

However, Bruck teaches wherein the video encoder performs luminance and chrominance filtering (col. 1, lines 59-col. 2, line 8).

Taking the teachings of Krishnamurthy, Adolph, and Bruck as a whole, it would have been obvious to one of ordinary skill in the art to modify the luminance and chrominance filtering of Bruck into Krishnamurthy and Adolph to improve the picture quality.

In response to the appellant arguments filed on 06/10/2008, the appellant argued that Bruck fails to overcome the deficiencies of Krishnamurthy, page 23.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the encoder (306 of fig. 3) for encoding video and audio stream based on the MPEG-2 standards, wherein the MPEG-2 standard would obviously have the luminance and chrominance filtering by Bruck (col. 1, lines 59-col. 2, line 8). Therefore, the combination of Krishnamurthy and Bruck make obvious the claimed invention.

7. Claims 14, 17-19, 27, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) in view of Hinchley et al. (US 6,490,250).

Re claims 14, 17, 27, and 30 , Krishnamurthy does not particularly disclose external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data; wherein the at least one bus interface is configurable to act as a bus master using direct memory access as claimed.

Hinchley teaches a first storage external to the device and a second storage external (108 and 116 of fig. 1) to the device (120 of figs. 1 and 2) and the at least one bus interface is configurable to act as a bus master (122 of fig. 1) using direct memory access (Note the bus (122) would obviously be the PCI bus and/or direct memory access, which serves the same purpose of transferring and receiving data to and from components within the circuit (100 of fig. 1).

Therefore, taking the teachings of Krishnamurthy, Adolph, and Hinchley, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages and random access memory with the interface bus (108, 116, and 122 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy and Adolph to provide an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed.

Re claims 18-19, 31-32, Krishnamurthy further teaches wherein the at least one bus interface (PCI BUS, 302 of fig. 3) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

8. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430), and further in view of Boice et al. (US 6,823,013).

Re claims 21-23, and 34-36, Krishnamurthy does not particularly disclose each of motion estimation processors comprises a plurality of search processors that operate in parallel upon a single macroblock, and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search) as claimed.

Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors subdividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of pixels blocks (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3)

Therefore, taking the teachings of Krishnamurthy, Adolph, and Boice as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the plurality of search processors (52 of fig. 4) of Boice into each of motion estimation processor of Krishnamurthy and Adolph to provide the process of motion estimation effectively reduces the temporal redundancy in successive video frames by exploiting the temporal correlation (similarities) that often exists between successive frames.

9. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) and Boice et al. (US 6,823,013), and further in view of Kopet et al. (US 5,448,310).

Re claim 23, the combination of Krishnamurthy, Adolph, and Boice teaches wherein the plurality of search processors operates in parallel upon a single macroblock, except each search processor operating at a different one of a plurality of resolutions as claimed.

However, Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29).

Taking the teachings of Krishnamurthy, Adolph, Boice, and Kopet as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Krishnamurthy Adolph, and Boice in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

10. Response to the Arguments filed on 10/10/2010. It is noted that the appellant's arguments filed 10/10/2010 have been fully considered but they are not persuasive.

The appellant noted that the Bruck (US 6,519,289) is not on any PTO-892 form in the remarks. The Bruck (US 6,519,289) is now in PTO-892 form of record.

I. The combination of Adolph and Hinchley

The appellant argued that the Office inconsistent in its identification of the aspect of Adolph that teaches the appellants' claimed invention as "first multiplexed stream". The appellant further argued that "MUX1" of Adolph produces "first multiplexed stream" and "MMUX" that also produces "first multiplexed stream".

It is noted that the appellants claim "**multiplexer circuitry** that operates in **a first mode** and **a second mode**, which when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video**, **first compressed audio**, **second compressed video**, and **second compressed audio**; and which when operating in **the second mode** concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**, and produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio.**"

The appellant admitted in the remarks page 17 that Appellants' claimed "first mode" and "second mode" characterize operation of Appellants' claimed "multiplexer circuitry," in which in the claimed "first mode," the "multiplexer circuitry" produces a "first multiplexed stream" using four components, namely, "first compressed video," "first compressed audio," "second compressed video," and second compressed audio." In the claimed "second mode," however, the claimed "multiplexer circuitry" produces the "first video stream" using the two components "first compressed video" and "second compressed video," and produces, in addition, a "second multiplexed stream" using the two components "second compressed video" and "second compressed audio." Thus, the "first mode" and "second mode" define the video and audio content of the "first multiplexed stream" and the "second multiplexed stream."

The examiner respectfully disagrees with the appellant. It is submitted that Adolph clearly teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream

from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

MODES	ADOLPH TEACHES
IN THE FIRST MODE: **multiplexer circuitry** that operates when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video**, **first compressed audio**, **second compressed video**, and **second compressed audio**	MMUX OF FIG. 3 using four components as VE1, AE1, VE2, and AE2 of fig. 3
IN THE SECOND MODE: concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**	MUX1 OF FIG. 3 using two components as VE1 and AE1 of fig. 3
IN THE SECOND MODE: produces **a second multiplexed stream** from **the second compressed video** and the **second**	MUX 2 OF FIG. 3 using two components as

compressed audio	VE2 and AE2 of fig. 3

It is noted that the appellant further argued that "MUX1" of Adolph produces "first multiplexed stream" and "MMUX" that also produces "first multiplexed stream". However, the appellant fails to show which "first multiplex stream" is produced in the first mode and which "first multiplexed stream" is produced in the second mode. As mentioned above, the claimed invention clearly states a first multiplexed stream is produced in the first mode and the first multiplexed is produced in the second mode concurrent with a second multiplexed stream. Adolph clearly teaches MMUX of fig. 3 produces a first multiplexed stream in the first mode, and MUX1 of fig. 3 concurrently produces the first multiplexed stream and MUX 3 of fig. 3 produces a second multiplexed stream in the second mode.

The appellant further argued that Adolph does not disclose transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio in the first mode or the first compressed video and first compressed audio in the second mode, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is

transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

The appellant repeatedly argued that Hinchley does not disclose any text to describe the claimed as specified in claim 10, and "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder".

The examiner respectfully disagrees with the appellant. It is submitted that the multiplexer circuitry of the present invention is disclosed in the specification in figure 5 as follows:

[0040] According to an embodiment of the present invention, device 100 is a parallel digital processor implemented on a single chip and designed for the purposes of real-time video/audio compression and multiplexing, MPEG-1 and MPEG-2 encoding.

[0061] Bitstream processor 112 encodes the compressed video data into a standard MPEG-1 and MPEG-2 format, in accordance with a sequence known in the art of encoding commands. Bitstream processor 112 transfers compressed video data streams to multiplexing processor 114.

[0063] Multiplexing processor 114 multiplexes the compressed video and the compressed audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of compressed video and/or audio and/or data.

[0064] Global controller 104 controls and schedules the video input buffer 102, the motion estimation processors 105 and 106, the digital signal processor 108, the memory controller 110, the bitstream processor 112, the 12C/GPIO interface, and the multiplexing processor 114. Global controller 104 is a central control unit that synchronizes and controls all of the internal chip units and communicates with all of the internal chip units using data-instruction-device buses.

The disclosure above encompass the claimed features as "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio".

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode

concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Let compare the multiplexing circuit of Hinchley and the present invention as follows:

Hinchley	The present invention

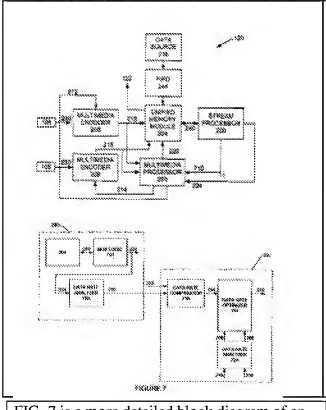
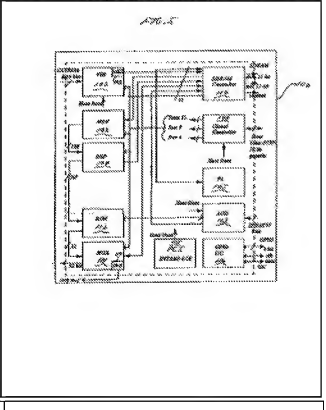

	

FIG. 7 is a more detailed block diagram of an embodiment of the stream processor 200 and multimedia processor 250 in accordance with the present invention. The stream processor 200 includes MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined multimedia stream 224. Combined multimedia stream 224 is preferably a program or transport stream as specified in MPEG2. The MUX logic 750	[0063] Multiplexing processor 114 multiplexes the compressed video and the compressed audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the

accesses the unified memory module 204 through data line 240 to retrieve the data and the instructions to perform on the data. After performing the required operations, the data 224 is temporarily written back to memory 204, for later transfer to the communications device 112 or other recipient of the Program or Transport Stream 224.	multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of compressed video and/or audio and/or data. This disclosure encompasses the claimed features

Based upon the comparison above, Hinchley's MUX logic (750 of fig. 7) has the same functions (MPEG2 standards) as Multiplexing processor (114 of fig. 5) of the present invention. Therefore, Hinchley teaches the claimed features.

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention. Therefore, the functions of MPEG-2 encoders (208 of fig. 2) of Hinchley meet the claimed features. Hinchley further teaches the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53). In view of the discussion above, the claimed invention is unpatentable over Adolph and Hinchley.

II. The combination of Adolph, Hinchley, and Ishihara.

The appellant argued that Adolph and Hinchley does not teach the features as specified in claims 10 and 24, therefore claims 21, 22, 34, and 35 are not taught by the combination of Adolph, Hinchley, and Ishihara.

The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the

performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX

logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention; and the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Ishihara teaches a plurality of search processors (7 of fig. 2) for performing motion analysis in parallel, each upon a different portion of a macroblock (PE1, PE2....PE33 of fig. 7; e.g. fig. 13). Therefore, one of ordinary skill in the art would have been obvious to modify the processor array (7 of fig. 2) of Ishihara into the motion estimation of the combination of Adolph and Hinchley to provide an improvement for reducing a hardware volume.

III. The combination of Adolph, Hinchley, Ishihara, and Kopet.

The appellant argued that Adolph and Hinchley does not teach the features as specified in claims 10 and 24, therefore claims 23 and 36 are not taught by the combination of Adolph, Hinchley, and Ishihara.

The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention; and the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation

coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29). Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Adolph, Hinchley, and Ishihara in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

IV The combination of Krishnamurthy and Adolph.

The appellant argued that the Office Action has not identify the required elements or suggestion or motivation to arrive at the required elements in the prior art sufficient to support such a purported rationale, pages 11-13 of the appeal brief.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) that comprises first encoder circuitry (306, ENC1 of fig. 3), second encoder circuitry (306, ENCn of fig. 3), multiplexer circuitry (308 of fig. 3), controller circuitry (304 of fig. 3), and at least one bus interface (302 of fig. 3); wherein the first encoder circuitry (306, ENC1 of fig. 3) comprises: a first video encoder (302 of fig. 3), a first audio encoder (322 of fig. 3), a first motion estimation processor (MPEG-2 encoder, 320 of fig. 2, would obviously comprise a motion estimation processor); wherein the second encoder circuitry (306, ENCn of fig. 3) comprises: a second video encoder (320 of fig. 3), a second motion estimation processor (320 of fig. 3, ENCn, MPEG-2 encoder obviously comprise a motion estimation processor), a second audio encoder (322, ENCn of fig. 3); wherein the multiplexer circuitry (308 of fig. 3) multiplexes the compressed video and audio outputs from the encoders (306 of fig. 3) to produce the multiplexed

signal, and the multiplexed signal is transmitted to circuitry external to the device (col. 19, lines 50-52, note the circuitry would obviously be a serial output port).

Krishnamurthy suggests models of encoders and multiplexer (fig. 3) will be useful for the advance allocation statistical multiplexer (e.g. 308 of fig. 3) that have mostly been developed for natural video and need modifications for game and web content. This is evidence to one skill in the art to use any suitable and conventional device to modify the statistical multiplexer (col. 15, lines 45-50).

Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second

multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Since Krishnamurthy and Adolph teach the video and audio signals accordance to MPEG standard and suggest modifications that would be made; therefore one skill of ordinary in the art would combined the suggested teachings of Krishnamurthy and Adolph to make obvious claimed invention.

Note not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. In re Preda, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F.2d 194, 138 USPQ 148 (CCPA 1963). Skill in the art is presumed. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). Furthermore, artisans must be presumed to know something about the art apart from what the references disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).

The obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969)). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge

generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Office Action above, paragraph 9, suggests all limitations to make obvious the claimed invention.

The appellant argued that the cited portion of Krishnamurthy in the Office Action does not teach " wherein the multiplexer circuitry operates in a first mode that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream coupled, and operates in a second mode that multiplexes the first compressed video and the first compressed audio to produce the first multiplexed stream and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream".

The examiner respectfully disagrees with the appellant. It is submitted that the multiplexer circuitry *(308 of fig. 3, note the stat-mux board can receive up to 24 different channels of transport bit-streams, col. 18, lines 50-52, from 24 encoders,306-306N of fig. 3, N=24, col. 18, line 15)*operates in a first mode *(col. 20, lines 22-26, "a multi-channel mode" would obviously be considered as a first mode, and the first mode is controlled by the overall board-level controls, col. 19, lines 39-42)* that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream *(Note the stat-mux, 308 of fig. 3, multiplexes up to 24 different channels of the transport bitstreams from 24 encoders, therefore the stat-mux would encompass to multiplex the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio as four different channels of transports of bitstreams.* and

operates in a mode that multiplexes the first compressed video and the first compressed audio to produce the first multiplexed stream *(326 of fig. 3, to multiplex the first compressed video and the first compressed audio to produce the first multiplexed stream)* and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream coupled via a second output *(326 of fig. 3, to multiplex the second compressed video and the second compressed audio to produce the first multiplexed stream; col. 19, lines 42-45, 328 of fig. 3, SSI of fig. 3).*

The appellant argued that Adolph does not teach the claimed features as specified in claim 10. The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream)

comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3. In view of the discussion above, the claimed invention is unpatentable over the combination of Krishnamurthy and Adolph.

The appellant further argued that the cited figure 3 of Krishnamurthy does not teach circuitry external to the device.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the outputs from the stat-mux are transmitted to circuitry *(col.19, lines 50-52, note the on-chip DMA will automatically move data from the TS output buffer of on-chip memory to the serial output port, this is evidence that the multiplexed compressed bitstreams are transmitted to the serial output port as circuitry)* external to the device (306 and 308 of fig. 3). It is noted that the circuitry external to the device is well known in the art and is taught by Hinchley *(Note the circuitry external (116 or 112 of fig. 1) to the device (120 of fig. 1, see also fig. 2).*

The appellant further argued that Krishnamurthy does not teach "a first output to circuitry external to the device", and "a second output to circuitry external to the device".

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the multiplexer, 308 of fig. 3, for outputting the multiplexed bitstream to circuitry external to the device by the output port (342 of fig. 3); this indicates that the output of the multiplexed bitstream must be transmitted to circuitry external to the device such as a

memory device or a communication device. It is noted that circuitry external from the single chip audio/video encoder device is well known in the art and is taught by Hinchley (figure 1, circuitry as 112 and 116, external to the device as 120).

The appellant further argued that Krishnamurthy does not teach, suggest, or render obvious controller circuitry that synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, harmonize, or orchestrate operation of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuit properly working.

Krishnamurthy further discloses Computer systems in accordance with the present invention avoid PCI bus delay by using the built-in multi-channel Synchronized Serial Interface (SSI) ports of multiple Digital Signal Processors (DSPs), where each DSP performs video and audio encoder control, PES/TS layer multiplexing, and computation of statistical measurements of its corresponding video stream payload. The DSPs' on-chip memories may also eliminate the need for bitstream First-In, First-Out (FIFO) chips and some common SDRAM (Synchronized Dynamic Random Access Memory) chips (col. 17, line 65-col. 18, line 8). There is CPLD (Complex Programmable Logic Device) or FPGA (Field-Programmable Gate Array) based deframing firmware to split the video and audio data, and to reproduce the video synchronization signals for the MPEG2 video encoder chip (col. 19, lines 18-22), the above disclosure is

evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

V. The combination of Krishnamurthy, Adolph, and Bruck.

The appellant argued that the combination of Krishnamurthy, Adolph, and Bruck doses teach the claimed features as specified in claims 13 and 26.

The examiner strongly disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Bruck teaches wherein the video encoder performs luminance and chrominance filtering (col. 1, lines 59-col. 2, line 8). Krishnamurthy teaches the encoder (306 of fig. 3) for encoding video and audio stream based on the MPEG-2 standards, wherein the MPEG-2 standard would obviously have the luminance and chrominance for filtering by Bruck (col. 1, lines 59-col. 2, line 8). Taking the teachings of Krishnamurthy, Adolph, and Bruck as a whole, it would have been obvious to one of ordinary skill in the art to modify the luminance and chrominance filtering of Bruck into Krishnamurthy and Adolph to improve the picture quality.

VI. The combination of Krishnamurthy, Adolph, and Hinchley

The appellant argued that the combination of Krishnamurthy, Adolph, and Hinchley doses teach the claimed features as specified in claims 14, 17-19, 27, 30-32.

The examiner respectfully disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above. Krishnamurthy further teaches wherein the at least one bus interface (PCI BUS, 302 of fig. 3) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer

circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

Hinchley teaches a first storage external to the device and a second storage external (108 and 116 of fig. 1) to the device (120 of figs. 1 and 2) and the at least one bus interface is configurable to act as a bus master (122 of fig. 1) using direct memory access (Note the bus (122) would obviously be the PCI bus and/or direct memory access, which serves the same purpose of transferring and receiving data to and from components within the circuit (100 of fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages and random access memory with the interface bus (108, 116, and 122 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy and Adolph to provide an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed. In view of the discussion above, the claimed invention is unpatentable over the combination of Krishnamurthy, Adolph, and Hinchley.

VII. The combination of Krishnamurthy, Adolph, and Boice

The appellant argued that the combination of Krishnamurthy, Adolph, and Boice doses teach the claimed features as specified in claims 21, 22, 24, and 35.

The examiner respectfully disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors subdividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a

single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of pixels blocks (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the plurality of search processors (52 of fig. 4) of Boice into each of motion estimation processor of Krishnamurthy and Adolph to provide the process of motion estimation effectively reduces the temporal redundancy in successive video frames by exploiting the temporal correlation (similarities) that often exists between successive frames.

VIII The combination of Krishnamurthy, Adolph, Boice, and Kopet

The appellant argued that the combination of Krishnamurthy, Adolph, and Boice doses teach the claimed features as specified in claims 21, 22, 24, and 35.

The examiner respectfully disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29). Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Krishnamurthy Adolph, and Boice in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

(10) Response to Argument

I. CLAIMS 10-20 AND 24-33 ARE UNPATENTABLE OVER THE COMBINATION OF ADOLPH AND HINCHLEY

A. Independent claims 10 and 24.

The appellant argued that the combination of Adolph and Hinchley fail to disclose or suggest multiplexer circuitry that operates in a first mode and a second mode in the manner required by claims 10 and 24, and Adolph does not disclose multiplexer circuitry that operates in a first mode and a second mode, which when operating in **the first mode** produces **a first multiplexed stream** from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in **the second mode** concurrently produces **the first multiplexed stream** from the first compressed video and the first compressed audio, and produces **a second multiplexed stream** from the second compressed video and the second compressed audio".

The examiner strongly disagrees with the appellant. It is submitted that Adolph clearly discloses which when **operating in the first mode (MMUX of fig. 3)** produces **a first multiplexed stream (the output of EMUX of fig. 3)** from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when **operating in the second mode** concurrently produces **the first multiplexed stream (MUX1 of fig. 3, the MUX1 clearly produces the multiplexed from the VE1 and AE1 as considered the first multiplexed stream)** from the first compressed video (VE1 of fig. 1) and the first compressed audio (VE1), and produces **a second multiplexed stream (MUX2 of fig. 2, the MUX1 produces the second**

multiplexed stream) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3). The appellant argued that the office is inconsistent interpretation of Adolph.

The appellant showed the office action by point out the following:

Non-Final Office Action dated 06/10/10	Final Office Action dated 11/16/10
Re claims 10 and 24, Adolph discloses a audio/video encoder device (fig. 3, a single device) comprising, on a single integrated circuit: multiplexer circuitry (MMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3);	The examiner respectfully disagrees with the applicant. It is submitted that Adolph clearly teaches multiplexer circuitry (MMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX 1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

The examiner strongly disagrees with the appellant. It is noted that the comparison above shows the non-final office action dated 6/10/10 and the final office action dated 10/16/10 that is consistent to disclose the first mode (MMUX of fig. 3) and the second mode (MUX1 and MUX 2 of fig. 3).

The appellant argued the Examiner alleges that two different elements of Adolph (that produce two different output signals, i.e., the output of "MUX 1" and the output of "MMUX"),

both teach producing Appellants' "first multiplexed stream." Appellants respectfully submit that the "programme data stream" output by "MUX 1" of Adolph cannot teach Appellants' claimed "first multiplexed stream," because the "MUX 1" does not have as inputs the "first compressed video," "second compressed video," "first compressed audio," and "second compressed audio," required by claim 10 "when operating in the first mode." The Examiner appears to be changing the element identified as teaching the claimed "first multiplexed stream" in the cited art to suit his needs, without explanation.

The examiner strongly disagrees with the appellant. It is noted that the claim recited "which when **operating in the first mode** produces **a first multiplexed stream** from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when **operating in the second mode** concurrently produces **the first multiplexed stream** from the first compressed video and the first compressed audio, and produces **a second multiplexed stream** from the second compressed video and the second compressed audio". The claimed invention clearly shows a first multiplexed stream is in the first mode, and the first multiplexed is in the second mode.

Adolph clearly discloses which when **operating in the first mode (MMUX of fig. 3)** produces **a first multiplexed stream (the output of EMUX of fig. 3)** from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when **operating in the second mode** concurrently produces **the first multiplexed stream (MUX1 of fig. 3, the MUX1 clearly produces the multiplexed from the VE1 and AE1 as**

considered the first multiplexed stream) from the first compressed video (VE1 of fig. 1) and the first compressed audio (VE1), and produces **a second multiplexed stream (MUX2 of fig. 2, the MUX1 produces the second multiplexed stream)** from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3). See the comparison below

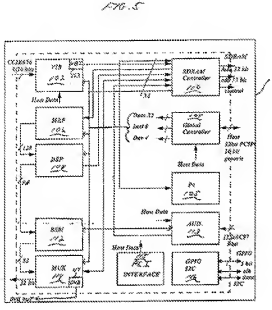
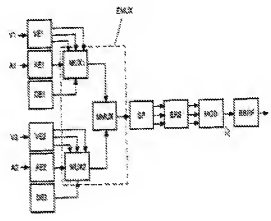
Appellant's Claim	ADOLPH TEACHES
IN THE FIRST MODE: **multiplexer circuitry** that operates when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video, first compressed audio, second compressed video**, and **second compressed audio**	MMUX OF FIG. 3 using four components as VE1, AE1, VE2, and AE2 of fig. 3
IN THE SECOND MODE: concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**	MUX1 OF FIG. 3 using two components as VE1 and AE1 of fig. 3
IN THE SECOND MODE: produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio**	MUX 2 OF FIG. 3 using two components as VE2 and AE2 of fig. 3

As consistency, the both office actions show Adolph teaches MUX1 produces **the first multiplexed stream** from **the first compressed video VE1** and **the first compressed audio AE1 and MUX 2 produces a second multiplexed stream** from **the second compressed video VE1** and the **second compressed audio AE2 in figure 3.**

The appellant argued that Adolph does not disclose transmits the first multiplexed stream to circuitry external to the device via a first output of the device, and transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

The examiner strongly disagrees with the appellant. Adolph teaches the first multiplexed stream is performed by MUX1 of figure 3 in the second mode, and the second multiplexed stream is performed by MUX2 of figure 3 in the second mode. The first multiplexed stream is transmitted to circuitry external to the device by the MMUX, SP, ERS, MOD, and BBRF of figure via a first output (the output MUX 1) of the device, and the second multiplexed stream is transmitted to circuitry external to the device by the MMUX, SP, ERS, MOD, and BBRF of figure via a first output (the output MUX 2) of the device. See comparison below.

Claim invention relies on figure 1, MUX 114	Aldolph

	 Fig.3
It is clear that the MUX 114 is outputting the first multiplexed stream and the second multiplexed stream to the circuitry external.	Adolph discloses the MMUX is outputting the first multiplexed stream from MUX1 and the second multiplexed stream from MUX2 to the circuitry external delivered by SP, ERS, MOD, and BBRF.

The appellant repeatedly argued that Hinchley does not disclose any text to describe the claimed as specified in claim 10, and "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder".

The examiner respectfully disagrees with the appellant. It is submitted that the multiplexer circuitry of the present invention is disclosed in the specification in figure 5 as follows: [0040] According to an embodiment of the present invention, device 100 is a parallel digital processor implemented on a single chip and designed for the purposes of real-time

video/audio compression and multiplexing, MPEG-1 and MPEG-2 encoding. [0061] Bitstream processor 112 encodes the compressed video data into a standard MPEG-1 and MPEG-2 format, in accordance with a sequence known in the art of encoding commands. Bitstream processor 112 transfers compressed video data streams to multiplexing processor 114. [0063] Multiplexing processor 114 multiplexes the compressed video and the compressed audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of compressed video and/or audio and/or data. [0064] Global controller 104 controls and schedules the video input buffer 102, the motion estimation processors 105 and 106, the digital signal processor 108, the memory controller 110, the bitstream processor 112, the 12C/GPIO interface, and the multiplexing processor 114. Global controller 104 is a central control unit that synchronizes and controls all of the internal chip units and communicates with all of the internal chip units using data-instruction-device buses.

The disclosure above encompasses the claimed features as "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first

compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio".

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Let compare the multiplexing circuit of Hinchley and the present invention as follows:

Hinchely	The present invention

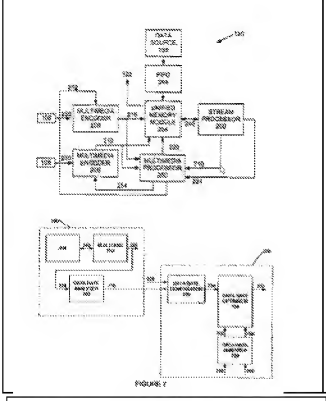
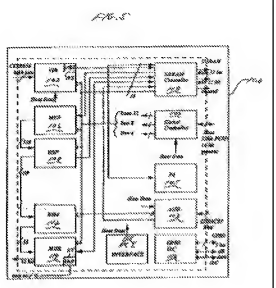

	

FIG. 7 is a more detailed block diagram of an embodiment of the stream processor 200 and multimedia processor 250 in accordance with the present invention. The stream processor 200 includes MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined multimedia stream 224. Combined multimedia stream 224 is preferably a program or transport stream as specified in MPEG2. The MUX logic 750 accesses the unified memory module 204 through data line 240 to retrieve the data and the instructions to perform on the data. After performing the required operations, the data 224 is temporarily written back to memory 204, for later transfer to the communications device 112 or other recipient of the Program or Transport Stream 224.	[0063] Multiplexing processor 114 multiplexes the compressed video and the compressed audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of compressed video and/or audio and/or data. This disclosure encompasses the claimed features

Based upon the comparison above, Hinchley's MUX logic (750 of fig. 7) has the same functions (MPEG2 standards) as Multiplexing processor (114 of fig. 5) of the present invention. Therefore, Hinchley teaches the claimed features.

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention. Therefore, the functions of MPEG-2 encoders (208 of fig. 2) of Hinchley meet the claimed features. Hinchley further teaches the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53). In view of the discussion above, the claimed invention is unpatentable over Adolph and Hinchley.

B. Claims 11-23 and 25-33.

II. Claims 21, 22, 34, and 35 are unpatentable over the combination of Adolph, Hinchley, and Ishihara.

The appellant argued that Adolph and Hinchley does not teach the features as specified in claims 10 and 24, therefore claims 21, 22, 34, and 35 are not taught by the combination of Adolph, Hinchley, and Ishihara.

The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when

operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode

produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention; and the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Ishihara teaches a plurality of search processors (7 of fig. 2) for performing motion analysis in parallel, each upon a different portion of a macroblock (PE1, PE2….PE33 of fig. 7; e.g. fig. 13). Therefore, one of ordinary skill in the art would have been obvious to modify the processor array (7 of fig. 2) of Ishihara into the motion estimation of the combination of Adolph and Hinchley to provide an improvement for reducing a hardware volume.

III. Claims 23 and 36 are unpatentable over Adolph, Hinchley, Ishihara, and Kopet

The appellant argued that Adolph and Hinchley does not teach the features as specified in claims 10 and 24, therefore claims 23 and 36 are not taught by the combination of Adolph, Hinchley, Ishihara, and Kopet.

The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that

operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention; and the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29). Therefore, it would have been obvious to one of ordinary skill in the art to

modify the teachings of Kopet into the combined motion estimation of Adolph, Hinchley, and Ishihara in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

IV. CLAIMS 1—12, 15-16, 20, 24-25, 28-29, AND 33 ARE UNPATENTABLE OVER KRISHNAMURTHY AND ADOLPH.

A. Independent Claims 10 and 24

The appellant repeatedly argued that the combination of Krishnamurthy and Adolph does not teach the claimed invention as shown in claims 10 and 24.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) that comprises first encoder circuitry (306, ENC1 of fig. 3), second encoder circuitry (306, ENCn of fig. 3), multiplexer circuitry (308 of fig. 3), controller circuitry (304 of fig. 3), and at least one bus interface (302 of fig. 3); wherein the first encoder circuitry (306, ENC1 of fig. 3) comprises: a first video encoder (302 of fig. 3), a first audio encoder (322 of fig. 3), a first motion estimation processor (MPEG-2 encoder, 320 of fig. 2, would obviously comprise a motion estimation processor); wherein the second encoder circuitry (306, ENCn of fig. 3) comprises: a second video encoder (320 of fig. 3), a second motion estimation processor (320 of fig. 3, ENCn, MPEG-2 encoder obviously comprise a motion estimation processor), a second audio encoder (322, ENCn of fig. 3); wherein the multiplexer circuitry (308 of fig. 3) multiplexes the compressed video and audio outputs from the encoders (306 of fig. 3) to produce the multiplexed signal, and the multiplexed signal is transmitted to circuitry external to the device (col. 19, lines 50-52, note the circuitry would obviously be a serial output port).

Krishnamurthy suggests models of encoders and multiplexer (fig. 3) will be useful for the advance allocation statistical multiplexer (e.g. 308 of fig. 3) that have mostly been developed for natural video and need modifications for game and web content. This is evidence to one skill in the art to use any suitable and conventional device to modify the statistical multiplexer (col. 15, lines 45-50).

Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed

audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Adolph further discloses as following:

Appellant's Claim	ADOLPH TEACHES
IN THE FIRST MODE: **multiplexer circuitry** that operates when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video, first compressed audio, second compressed video**, and **second compressed audio**	MMUX OF FIG. 3 using four components as VE1, AE1, VE2, and AE2 of fig. 3
IN THE SECOND MODE: concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**	MUX1 OF FIG. 3 using two components as VE1 and AE1 of fig. 3
IN THE SECOND MODE: produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio**	MUX 2 OF FIG. 3 using two components as VE2 and AE2 of fig. 3

Adolph teaches MUX1 produces **the first multiplexed stream** from **the first compressed video VE1** and **the first compressed audio AE1 and MUX 2 produces a second**

multiplexed stream from **the second compressed video VE1** and the **second compressed audio AE2 in figure 3.**

Since Krishnamurthy and Adolph teach the video and audio signals accordance to MPEG standard and suggest modifications that would be made; therefore one skill of ordinary in the art would combined the suggested teachings of Krishnamurthy and Adolph to make obvious claimed invention.

Note not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. In re Preda, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F.2d 194, 138 USPQ 148 (CCPA 1963). Skill in the art is presumed. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). Furthermore, artisans must be presumed to know something about the art apart from what the references disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).

The obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969)). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Office Action above, paragraph 9, suggests all limitations to make obvious the claimed invention.

The appellant further argued that the cited portion of Krishnamurthy in the Office Action does not teach " wherein the multiplexer circuitry operates in a first mode that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream coupled, and operates in a second mode that multiplexes the first compressed video and the first compressed audio to produce the first multiplexed stream and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream".

The examiner respectfully disagrees with the appellant. It is submitted that the multiplexer circuitry (308 of fig. 3, note the stat-mux board can receive up to 24 different channels of transport bit-streams, col. 18, lines 50-52, from 24 encoders,306-306N of fig. 3, N=24, col. 18, line 15)operates in a first mode (col. 20, lines 22-26, "a multi-channel mode" would obviously be considered as a first mode, and the first mode is controlled by the overall board-level controls, col. 19, lines 39-42) that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream (Note the stat-mux, 308 of fig. 3, multiplexes up to 24 different channels of the transport bitstreams from 24 encoders, therefore the stat-mux would encompass to multiplex the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio as four different channels of transports of bitstreams. and operates in a mode that multiplexes the first compressed video and the first compressed audio to

produce the first multiplexed stream (326 of fig. 3, to multiplex the first compressed video and the first compressed audio to produce the first multiplexed stream) and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream coupled via a second output (326 of fig. 3, to multiplex the second compressed video and the second compressed audio to produce the first multiplexed stream; col. 19, lines 42-45, 328 of fig. 3, SSI of fig. 3).

The appellant repeatedly argued that Adolph does not teach the claimed features as specified in claim 10.

The examiner strongly disagrees with the appellant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first

multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3. In view of the discussion above, the claimed invention is unpatentable over the combination of Krishnamurthy and Adolph.

The appellant further argued that the cited figure 3 of Krishnamurthy does not teach circuitry external to the device.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the outputs from the stat-mux are transmitted to circuitry (col.19, lines 50-52, note the on-chip DMA will automatically move data from the TS output buffer of on-chip memory to the serial output port, this is evidence that the multiplexed compressed bitstreams are transmitted to the serial output port as circuitry) external to the device (306 and 308 of fig. 3). It is noted that the circuitry external to the device is well known in the art and is taught by Hinchley (Note the circuitry external (116 or 112 of fig. 1) to the device (120 of fig. 1, see also fig. 2).

The appellant further argued that Krishnamurthy does not teach "a first output to circuitry external to the device", and "a second output to circuitry external to the device".

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches the multiplexer, 308 of fig. 3, for outputting the multiplexed bitstream to circuitry external to the device by the output port (342 of fig. 3); this indicates that the output of the multiplexed bitstream must be transmitted to circuitry external to the device such as a

memory device or a communication device. It is noted that circuitry external from the single chip audio/video encoder device is well known in the art and is taught by Hinchley (figure 1, circuitry as 112 and 116, external to the device as 120).

The appellant further argued that Krishnamurthy does not teach, suggest, or render obvious controller circuitry that synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

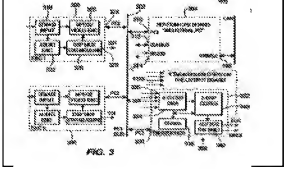
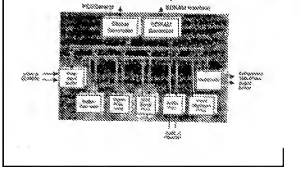
The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, harmonize, or orchestrate operation of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuit properly working.

Krishnamurthy further discloses Computer systems in accordance with the present invention avoid PCI bus delay by using the built-in multi-channel Synchronized Serial Interface (SSI) ports of multiple Digital Signal Processors (DSPs), where each DSP performs video and audio encoder control, PES/TS layer multiplexing, and computation of statistical measurements of its corresponding video stream payload. The DSPs' on-chip memories may also eliminate the need for bitstream First-In, First-Out (FIFO) chips and some common SDRAM (Synchronized Dynamic Random Access Memory) chips (col. 17, line 65-col. 18, line 8). There is CPLD (Complex Programmable Logic Device) or FPGA (Field-Programmable Gate Array) based deframing firmware to split the video and audio data, and to reproduce the video synchronization signals for the MPEG2 video encoder chip (col. 19, lines 18-22), the above disclosure is

evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

The appellant repeatedly argued that the Office Action fails to identify any portion of text of Krishnamurthy teaches "multiplexing circuit" for operating in a first mode and second mode, the first multiplexed stream coupled via the fist output to circuitry external to the device, a second multiplexed stream coupled to via second output to circuitry external to the device, single chip video/audio encoder device, the controller circuitry synchronizes operation of the first encoder circuitry, the second encoder circuitry, and the multiplexer circuitry, pages 13-21 of the remarks.

The examiner respectfully disagrees with the appellant. It is submitted that Krishnamurthy teaches a single audio/video encoder device (fig. 3) that is the same as the described single audio/video device of the present invention as follows:

Krishnamurthy	The present invention relies on 60/296,766
	

Krishnamurthy teaches a first MPEG-2 video encoder (320), a first audio encoder (322), a second MPEG-2 encoder (320n, 306n), a second audio encoder (322n, 306n), and a statistical multiplexing board (308), wherein the statistical multiplexing board (308 of fig. 3) would

obviously be considered as a multiplexing circuit for multiplexing the first encoded video signal and the first encoded audio signal (SSI, 328, 336), and the second encoded video signal and the second encoded audio signal (SSI, 328n, 336), the stat-mux can multiplex up to 24 channels of low delay MPEG-2 video/audio input bitstreams (SSI of fig. 3, col. 18, lines 50-52; col. 20, lines 10-11), and each SSI has three wires carrying a clock signal (sclk), a data signal (sdat), and a frame signal (col. 20, lines 12-13), and the frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters (col. 20, lines 22-25), so this disclosure would fairly suggest that the stat-mux (308) multiplexing the first encoded video and audio in a first mode and the second encode video and audio in a second mode.

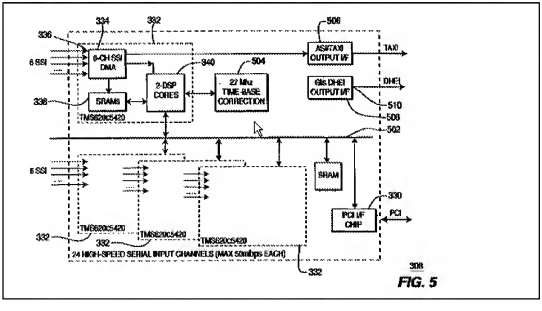


FIG. 5

Krishnamurthy further teaches the stat-mux in figure 5 for outputting the multiplexed stream of the first encoded video and the first encoded video to circuitry external to the device (506, col. 20, lines 27-28), wherein the stat-mux would obviously output the multiplexed stream

of the second encoded video and the second encoded audio to circuitry external to the device (506; col. 20, lines 27-28).

Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would obviously synchronize operation of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuit properly working.

Adolph teaches which when **operating in the first mode (MMUX of fig. 3)** produces **a first multiplexed stream (the output of EMUX of fig. 3)** from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when **operating in the second mode** concurrently produces **the first multiplexed stream (MUX1 of fig. 3, the MUX1 clearly produces the multiplexed from the VE1 and AE1 as considered the first multiplexed stream)** from the first compressed video (VE1 of fig. 1) and the first compressed audio (VE1), and produces **a second multiplexed stream (MUX2 of fig. 2, the MUX1 produces the second multiplexed stream)** from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3). Therefore, one skill in the art would have been obvious to modify the teachings of Adolph into Krishnamurthy to make obvious claimed invention.

B. Claims 10-12, 15-16, 20, 24-25, and 33

V. The combination of Krishnamurthy, Adolph, and Bruck teaches all limitations in claims 13 and 26.

The appellant argued that the combination of Krishnamurthy, Adolph, and Bruck does not teach the claimed features as specified in claims 13 and 26.

The examiner strongly disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Bruck teaches wherein the video encoder performs luminance and chrominance filtering (col. 1, lines 59-col. 2, line 8). Krishnamurthy teaches the encoder (306 of fig. 3) for encoding video and audio stream based on the MPEG-2 standards, wherein the MPEG-2 standard would obviously have the luminance and chrominance for filtering by Bruck (col. 1, lines 59-col. 2, line 8). Taking the teachings of Krishnamurthy, Adolph, and Bruck as a whole, it would have been obvious to one of ordinary skill in the art to modify the luminance and chrominance filtering of Bruck into Krishnamurthy and Adolph to improve the picture quality.

VI. The combination of Krishnamurthy, Adolph, and Hinchley teaches claim 14, 17-19, 27, and 30-32.

The appellant argued that the combination of Krishnamurthy, Adolph, and Hinchley doses teach the claimed features as specified in claims 14, 17-19, 27, 30-32.

The examiner respectfully disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above. Krishnamurthy further teaches wherein the at least one bus interface (PCI BUS, 302 of fig. 3) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface

("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

Hinchley teaches a first storage external to the device and a second storage external (108 and 116 of fig. 1) to the device (120 of figs. 1 and 2) and the at least one bus interface is configurable to act as a bus master (122 of fig. 1) using direct memory access (Note the bus (122) would obviously be the PCI bus and/or direct memory access, which serves the same purpose of transferring and receiving data to and from components within the circuit (100 of fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages and random access memory with the interface bus (108, 116, and 122 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy and Adolph to provide an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed. In view of the discussion above, the claimed invention is unpatentable over the combination of Krishnamurthy, Adolph, and Hinchley.

VII. The combination of Krishnamurthy, Adolph, and Boice teaches claims 21, 22, 34, and 35.

The appellant argued that the combination of Krishnamurthy, Adolph, and Boice does not teach the claimed features as specified in claims 21, 22, 24, and 35.

The examiner respectfully disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors subdividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a

single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of pixels blocks (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the plurality of search processors (52 of fig. 4) of Boice into each of motion estimation processor of Krishnamurthy and Adolph to provide the process of motion estimation effectively reduces the temporal redundancy in successive video frames by exploiting the temporal correlation (similarities) that often exists between successive frames.

VIII. The combination of Krishnamurthy, Adolph, Boice, and Kopet teaches claims 21-22, 23, and 34-35.

The appellant argued that the combination of Krishnamurthy, Adolph, and Boice doses teach the claimed features as specified in claims 21, 22, 34, and 35.

The examiner respectfully disagrees with the appellant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29). Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Krishnamurthy Adolph, and Boice in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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